

YOR920010565US2

filed with the parent application are attached to a copy of the originally filed specification which are included herewith.

IN THE CLAIMS:

Please cancel claims 1-10 without prejudice or disclaimer.

11. (Original) A method of forming a metal-insulator-metal capacitor and an associated semiconductor transistor having a metal gate, said method comprising:

forming a first metal layer;

forming an insulator over said first metal layer;

removing a portion of said first metal layer from a gate region; and

forming a second metal layer over said insulator and in said gate region,

wherein said second metal layer comprises a gate of said transistor and a plate of said transistor.

12. (Original) The method in claim 11, further comprising forming sidewall spacers adjacent sacrificial gate structures, wherein said first metal layer is formed over said sidewall spacers.

13. (Original) The method in claim 11, further comprising, after said forming of said sidewall spacers, doping source and drain regions in said substrate.

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14. (Original) The method in claim 11, further comprising planarizing said first metal layer.
15. (Original) The method in claim 14, wherein said planarizing of said first metal layer reduces voids and surface irregularities in said second metal layer.
16. (Original) The method in claim 11, further comprising forming an insulator over said first metal layer.
17. (Original) The method in claim 16, wherein said insulator comprises both a capacitor insulator and a gate insulator.
18. (Original) The method in claim 11, wherein said plate comprises an upper plate of said capacitor.
19. (Original) A method of forming a metal-insulator-metal capacitor and an associated semiconductor transistor having a metal gate, said method comprising:
 - patterning sacrificial gate structures over a substrate;
 - forming sidewall spacers adjacent said sacrificial gate structures;
 - forming a first metal layer adjacent said sidewall spacers;
 - planarizing said first metal layer;
 - removing said sacrificial gate structures;
 - forming an insulator over said first metal layer;

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removing a portion of said first metal layer from a gate region; and
forming a second metal layer over said insulator and in said gate region,
wherein said second metal layer comprises a gate of said transistor and a plate of said
transistor.

20. (Original) The method in claim 19, wherein said planarizing of said first metal layer
reduces voids and surface irregularities in said second metal layer.

21. (Original) The method in claim 19, wherein said insulator comprises both a capacitor
insulator and a gate insulator.

22. (Original) The method in claim 19, further comprising, after said forming of said
sidewall spacers, doping source and drain regions in said substrate.

23. (Original) The method in claim 21, wherein said plate comprises an upper plate of
said capacitor.